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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/672,758 | 09/27/2003 | Carl E. Love | BEA920020005US1 | 1034 |

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| EXAMINER | |
|---|---|
| URICK, MATTHEW T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2113 | |

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/672,758 | LOVE ET AL. | |
| | Examiner | Art Unit | |
| | Matt Urick | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19 and 20* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Non-Final Official Action***

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Coon (United States Patent 6,356,615).

As per claim 1, Coon discloses:

A hardware counter comprising:

a memory array storing a plurality of counter values (column 5 line 65 – column 6 line 5) indexable by an index constructed based at least on a number of a plurality of events to which the counter values correspond (column 5 lines 20-24: signal combiners may define what criteria the counters respond to) ; and,

a hardware incrementer to read the counter values from the memory array by values of the index, increment the counter values, and write the counter values as incremented back into the memory array (column 5 line 65 – column 6 line 5: counters may be decremented according to inputs; column 1 lines 13-21: counters may increment or decrement, and may be implemented has hardware (hard-wiring) or software).

As per claim 2, Coon discloses:

The hardware counter of claim 1, wherein the index is constructed as a number of bits binarily representing the number of the plurality of events (column 6 lines 16-30).

As per claim 3, Coon discloses:

The hardware counter of claim 1, wherein the index is constructed further based on a number of a plurality of qualifiers to the plurality of events (column 6 lines 16-30: any Boolean logic combination of the inputs may be used as a qualifier).

As per claim 4, Coon discloses:

The hardware counter of claim 3, wherein the index is constructed as a concatenation of a number of bits binarily representing the number of the plurality of events and a number of bits binarily representing the number of the plurality of qualifiers, such that each counter value corresponds to a unique combination of one of the plurality of events and one of the plurality of qualifiers (column 7 lines 58-62: there are enough Boolean logic combinations available that a unique set of operations may be used for each of the counters with several combinations left over).

As per claim 5, Coon discloses:

The hardware counter of claim 3, wherein the index is constructed as a number of bits binarily representing a number of possibly occurring event-and-qualifier combinations, such that each counter value corresponds to a different one of the

possibly occurring event-and-qualifier combinations (column 7 lines 58-62 as applied in claim 4), wherein a number of counter values is less than the number of the plurality of events multiplied by the number of the plurality of qualifiers (figure 1: four counters (3, 5, 7, 9) depicted. Column 10 lines 55-61: a 32 bit word may be used to count the number of events. The number of events counted in a 32 bit register multiplied by any number of chosen qualifiers will be greater than the number of counter values (four counter values are depicted in figure 1)).

As per claim 6, Coon discloses:

The hardware counter of claim 5, further comprising index generation hardware to generate a value of the index for an input one of the possibly occurring event-and-qualifier combinations (column 6 lines 16-30: C programming (software) or a series of MUXs (hardware) may be used).

As per claim 7, Coon discloses:

The hardware counter of claim 1, wherein the hardware incrementer comprises a hardware adder that adds an increment value to the counter values, such that results of adding the increment value to the counter values is written back into the memory array (column 5 line 65 – column 6 line 5: counters may be decremented according to inputs; column 1 lines 13-21: counters may increment or decrement, and may be implemented has hardware (hard-wiring) or software).

As per claim 8, Coon discloses:

The hardware counter of claim 7, wherein the hardware incrementer further comprises a register storing the increment value (column 1 lines 24-36).

As per claim 9, Coon discloses:

The hardware counter of claim 1, further comprising:

index generation hardware to generate the index (column 6 lines 16-30: C programming (software) or a series of MUXs (hardware) may be used).; and,

hardware to read the counter values from the memory array by the values of the index and write the counter values to the memory array (column 5 line 65 – column 6 line 5: counters may be decremented according to inputs; column 1 lines 13-21: counters may increment or decrement, and may be implemented has hardware (hard-wiring) or software).

As per claim 10, Coon discloses:

The hardware counter of claim 1, wherein the memory array is divided into a plurality of memory banks over which the plurality of counter values are stored, each memory bank having a separate instance of the hardware incrementer (column 5 line 65 – column 6 line 5).

As per claim 11, Coon discloses:

The hardware counter of claim 10, wherein the index globally indexes the plurality of counter values over the plurality of memory banks as a whole (column 5 lines 20-24).

As per claim 12, Coon discloses:

The hardware counter of claim 10, wherein each memory bank has a separate instance of the index that indexes only those of the plurality of counters stored in the memory bank, each memory bank having associated therewith index generation hardware to generate the separate instance of the index for the memory bank (column 5 lines 20-24).

As per claim 13, Coon discloses:

A method comprising:

generating via hardware a value of an index based on one of a plurality of events (column 5 lines 20-24: signal combiners may define what criteria the counters respond to; column 1 lines 13-21: counters may increment or decrement, and may be implemented has hardware (hard-wiring) or software), a count value for an occurrence of which is to be incremented (column 5 line 65 – column 6 line 5);

reading by the value of the index the counter value from a memory array indexed by the index (column 5 line 65 – column 6 line 5: counters may be decremented according to inputs);

incrementing via hardware the counter value (column 5 line 65 – column 6 line 5: counters may be decremented according to inputs; column 1 lines 13-21: counters may increment or decrement); and,

writing the counter value as incremented back into the memory array (column 5 line 65 – column 6 line 5: counters may be decremented according to inputs; column 1 lines 13-21: counters may increment or decrement).

As per claim 14, Coon discloses:

The method of claim 13, wherein generating via hardware the value of the index comprises generating via hardware the value of the index based on the one of the plurality of events and one of a plurality of qualifiers to the events (column 6 lines 16-30: any Boolean logic combination of the inputs may be used as a qualifier).

As per claim 15, Coon discloses:

The method of claim 14, wherein generating via hardware the value of the index comprises generating the index as one of:

a concatenation of a number of bits binarily representing the number of the plurality of events and a number of bits binarily representing the number of the plurality of qualifiers (column 6 lines 16-30: any Boolean logic combination of the inputs may be used as a qualifier); and,

a number of bits binarily representing a number of possibly occurring event-and-qualifier combinations, such that each counter value corresponds to a different one of

the possibly occurring event-and-qualifier combinations (column 7 lines 58-62: there are enough Boolean logic combinations available that a unique set of operations may be used for each of the counters with several combinations left over).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coon (United States Patent 6,356,615) in view of Intel ("Intel News Release" (c) 1995, Intel Corporation).

As per claim 16, Coon discloses:

a processor and a performance counter operatively coupled to the processor to count occurrences of events (column 5 line 65- column 6 line 5),

the performance counter having a lesser number of hardware incrementers than a number of the events of which the performance counter counts the occurrences (column 5 lines 29-30, 54-67, column 7 lines 46-53: Each counter may monitor a number of different events).

Coon does not disclose:

A system comprising a plurality of nodes, each node having a processor and a performance counter.

Intel discloses that the P6 (AKA Pentium Pro) line of processors is capable of being implemented in a multiprocessor environment (page 2, section titled "Additional Features"). Intel discloses that this environment enables the processor to work with more reliability and efficiency. Coon discloses that his invention can be run on the Pentium Pro line of processors (column 1 lines 30-36), and that the object is to analyze performance and reliability (column 1 lines 5-10). Coon also discloses that the counter may use registers on the processor (column 1 lines 30-36), so each processor may contain its own counter. Coon's system could be used in the multiprocessor environment as disclosed by Intel to take advantage of the increased reliability and performance of the Pentium Pro line of processors. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate multiple processors into the event counter of Coon, increasing reliability and performance.

As per claim 17, Coon discloses:

The system of claim 16, wherein the performance counter counts occurrences of combinations of events and qualifiers, the performance counter having a lesser number of the hardware incrementers than a number of the combinations of the events and the qualifiers of which the performance counter counts the occurrences (column 5 lines 29-30, 54-67, column 7 lines 46-53: Each counter may monitor a number of different

events, as well as Boolean logic combinations of events).

As per claim 19, Coon discloses:

The system of claim 16, wherein

the performance counter comprises a plurality of memory banks and a plurality of hardware incrementers corresponding to the memory banks (column 5 line 65- column 6 line 5),

each memory bank storing counter values for counting the occurrences of some of the events (column 5 line 65- column 6 line 5),

each hardware incrementer incrementing the counter values of the memory bank to which the hardware incrementer corresponds in response to the occurrences of the some of the events to which the counter values of the hardware incrementer correspond (column 5 line 65- column 6 line 5).

As per claim 20, Coon fails to disclose:

The system of claim 16, wherein each node further comprises memory that is local to the processor of the node and remote to the processor of every other of the nodes.

Intel discloses that the P6 (AKA Pentium Pro) line of processors is capable of being implemented in a multiprocessor environment (page 2, section titled "Additional Features"). Intel discloses that this environment enables the processor to work with more reliability and efficiency. Coon discloses that his invention can be run on the

Pentium Pro line of processors (column 1 lines 30-36), and that the object is to analyze performance and reliability (column 1 lines 5-10). Coon also discloses that the counter may use registers on the processor (column 1 lines 30-36), so each counter's memory would be local to the processor and remote to every other processor in the system. Coon's system could be used in the multiprocessor environment as disclosed by Intel to take advantage of the increased reliability and performance of the Pentium Pro line of processors. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate multiple processors into the event counter of Coon, increasing reliability and performance.

***Allowable Subject Matter***

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 18 states:

The system of claim 16, wherein the performance counter comprises a memory array storing counter values for counting the occurrences of the events, and a single hardware incrementer to increment the counter values of the memory array in response to the occurrences of the events to which the counter values correspond.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matt Urick whose telephone number is (571) 272-0805. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Robert W Beausoliel

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